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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,777	01/14/2004	Chih Chieh Yeh	681939-62US	3578

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2005 MARKET STREET, SUITE 2200
PHILADELPHIA, PA 19103

EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,777	YEH ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-10 and 21-30* is/are allowed.

6)☒ Claim(s) *1-5 and 11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Information Disclosure Statement submitted by Applicant on January 14, 2004 have been received and fully considered.

2. The disclosure is objected to because of the following informalities:

In claim 2, line 3, one of the two "." should be deleted.

Appropriate correction is required.

3. Claims 6-10 are objected to as failing to provide proper antecedent basis for the claimed subject matter. Claim 6 recites the limitation "the nitride layer" in line 4. There is insufficient antecedent basis for this limitation in the claim.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-5, 11-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 5, 7, 8, 28, 32-33 of U.S. Patent No. 6,690,601 (hereinafter U.S. Pat No. '601) in view of Sudo et al. (U.S. Patent No. 5,659,503).

Claims 1 and 28 of U.S. Pat. No. '601 recited a trapping non-volatile memory cell comprising a P-type semiconductor substrate comprising a source, a drain spaced from

the source, and a channel formed between the source and the drain, a tunnel layer overlaying the channel, a first isolation layer overlaying the tunnel layer, a nonconducting charge trapping layer overlaying the first isolation layer, a second isolation overlaying the nonconducting charge trapping layer, wherein charge trapping layer receiving and retaining electrons in an erase state for the memory cell, and receiving electric hole injection in a programming state so that the net charge of the nonconducting charge trapping layer is reduced in the programming state. Claims 1 and 28 of U.S. Pat. No. '601 did not recite the comparator

Sudo et al. disclosed in Figure 1 a prior art nonvolatile memory device having a memory cell array [1] including a plurality of floating memory cells, wherein in erase operation, the electrons are injected into the floating gate of the memory cells (column 3, lines 25-41). Sudo et al. further disclosed the memory device including a comparing circuits [8] to compare the voltage [Vrd] of the selected bit lines with a reference voltage [Vref] so that the content stored in the selected memory cell transistor can be discriminated (column 4, lines 7-10).

Regarding claim 1, 16, 19 of the present application, it would have been obvious to a person of ordinary skill in the art to modify the trapping nonvolatile memory in claims 1 and 28 of U.S. Pat. No. '601 by providing the comparing circuit of Sudo et al..

The rationale is as follows: A person of ordinary skill in the art would have been motivated to used the compare circuit of Sudo et al. to accurately determine the content stored in the memory cell in a read operation.

Regarding claim 2 of the present application, claim 1 of U.S. Pat. No. '601 recited the charge trapping layer receiving and retaining electrons in an erase state, which inherently increases the threshold voltage of the erased cell, which leads to the voltage threshold of erased cell is higher the threshold voltage of the programmed cell.

Regarding claim 3 of the present application, since the charge trapping layer in claim 1 of U.S. Pat. No. '601 receiving and retaining electrons in erase state, and receiving hole injection in program state, the amount of electrons accumulated in the charge trapping layer is higher in the erase state than in the programmed state, which inherently causes the current in the erase state is lower than in the programmed state.

Regarding claim 4 of the present application, claim 5 of U.S Pat. No. '601 recited the first and second isolation layer are mode of silicon oxide.

Regarding claim 5 of the present application, claim 33 of U.S. Pat No. '601 recited the nonconducting charge trapping layer is made of nitride.

Regarding claim 11 of the present application, claim 13 of U.S. Pat. No. '601 recited two bits of the memory cell are programmed.

Regarding claim 12 of the present application, as electric hole injected into the charge trapping layer when the memory cell is programmed, it is inherent that the net charge of the charge regions is reduced.

Regarding claims 13-14 of the present application, claim 7 of U.S. Pat. '601 recited a tunnel layer between the channel region and the first isolation layer, the tunnel layer overlying the channel region, wherein the tunnel layer includes energy barrier for electrons and electric holes which are lower than those of the first isolation layer.

Regarding claims 17-18, since the amount of electrons trapped in the charge trapping layer is different in the erased state and the programmed state which inherently yields the current in the erased state differs from the current in the programmed state, it would have been obvious to modify the memory device in claim 1 of U.S. Pat. No. '601 to provide a reference voltage which has magnitude between the current of the erased state and programmed state.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to use the reference current to accurately detect whether the memory cell is in erases state or the programmed state.

Regarding claims 15, 20 of the present application, claim 8 of U.S> Pat No. '601 recited the tunnel layer is made of one selected from the group consisting of titanium oxide and BST (barium, strontium, and tantalum compound).

6. Claims 6-10 and 21-30 are allowed.

7. The following is an examiner's statement of reasons for allowance:

The prior art failed to show or suggest the trapping layer being operable to retain electrons in an erase state for one of a drain bit and the source bit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawakami is cited to show a memory device having reference cell coupled to a sense amplifier, Hirano is cited to show memory device having electrons injected into the floating gate in erase operation.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:oo PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
September 06, 2005